Silicon-on-Sapphire MOSFET Distributed Amplifier with Coplanar Waveguide Matching

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Abstract

Analog application of silicon RF MOSFET circuits have received increased attention as potentially lower cost and higher integration alternatives to III-V technology. In this work, a thin-film silicon-on-sapphire (SOS) n-MOSFET based distributed amplifier is demonstrated. Impedance matching was achieved by a coplanar waveguide (CPW) on sapphire. The distributed amplifier has a bandwidth of 10 GHz and 5dB gain. The amplifier's bandwidth is the broadest ever reported for a Si MOSFET technology.

Introduction

Distributed amplifiers are used in wide-band, high-data-rate optical communications and in a variety of high-frequency instruments. Increasing attention is being given to such circuit implemented in silicon, because of its potential for reduced cost and the possibility of higher integration to further reduce the size and cost of the overall system.

In this work, a monolithic integrated distributed amplifier implemented with silicon on sapphire (SOS) technology is reported. Thin film SOS technology has been shown to be suitable for high frequency circuits as a result the high frequency response of the transistors and the low loss substrate. [1] This enables circuit approaches well proven in GaAs technology to be used.

Silicon on Sapphire Technology

The silicon on sapphire (SOS) MOSFETs are fabricated on mesa isolated 1000Å thick film silicon islands on a sapphire substrate. Their f_T and f_{max} were 21 and 50 GHz respectively. Optical projection lithography was used to define the gates, which were 0.5µm long. After gate and silicide formation and several planarization steps, the titanium silicide gate was uncovered and re-enforced with Al first level metal (Aluminum T-gate). The addition of the aluminum T-gates reduces the gate resistance to improve the f_{max} of the SOS MOSFETs. With the exception of the T-gate step, conventional digital IC processes were utilized. The cross-section of the SOS thin film MOSFET devices are shown in figure 1.

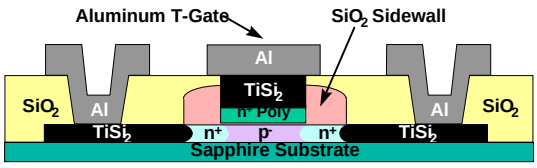

Figure 1. Cross-section of the SOS Thin Film MOSFET

Coplanar transmission lines were implemented using Al interconnect lines deposited on sapphire. The total Al thickness was 2.1µm thick (0.5µm for the first metal and 1.6µm for the second metal), resulting a sheet resistance of 0.02Ω/□. By increasing the Al thickness, it is believed that the amplifier performance can be further increased.

Circuit Design

a. Distributed amplifier design

The distributed amplifier's input and output lines were designed to behave as transmission lines of 50Ω characteristic impedance. In these lines, the input and output impedance of the MOSFETs is absorbed in the distributed structure composed of higher impedance transmission lines. By doing so, the

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

amplifiers can exhibit wide bandwidth to nearly $f_T/2$ or up to the limits imposed by transmission line resistive losses. The circuit schematic diagram is shown in figure 2.

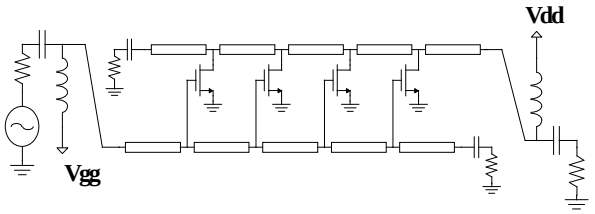

Figure 2. Schematic diagram of the SOS Thin Film MOSFET distributed amplifier

Preliminary design used the simple $Z_0 = \sqrt{L/C}$ definition for a characteristic impedance of a transmission line, combining the input and output capacitance Cgs (gate-source capacitance) and Cds (drain-source capacitance) with the capacitance per length of the waveguides to achieve the desired 50Ω impedances. The line impedance and length then were optimized by SPICE simulation such that the delay at each stage of the amplifier is the same.

Further simulation were carried out in HP EEsof Libra. The model used for the MOSFET simulation was the SPICE level 3 model. The values for the device model for a 100µm device are shown in table 1.

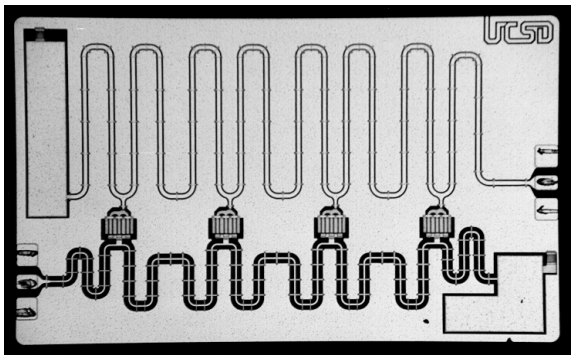

Figure 3. Photograph of a distributed amplifier with on chip termination

Gate width per stage was 300µm. Gate length of the MOSFETs was 0.5µm. Four stages were used. The input and output impedances of the MOSFETs correspond closely to Cgs = 0.6 fF and Cds = 0.22fF per micron gate width. In addition Rg (series gate resistance) of 4Ω, Rd (series drain resistance) of 10Ω, and gm of 100mS/mm were used in the simulation. A photograph of the fabricated circuit is shown in figure 3.

b. SOS coplanar waveguide (CPW) design

Coplanar waveguides were used as inductive elements to match to the input capacitance of the SOS MOSFETs. The low loss substrate of the silicon-on-sapphire technology is an important advantage over conventional bulk silicon technology for the realization of these waveguides. This property improves the quality factor, Q, for the passive elements, such as inductors, capacitors, and waveguides [3]. These high Q on-chip matching elements are essential for the design of the distributed amplifier in the gigahertz range [3].

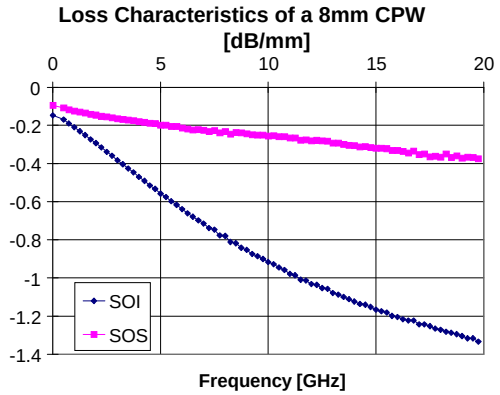

Figure 4. Comparison of loss characteristic of 50Ohm coplanar waveguides on bulk CMOS and sapphire

A comparison of the coplanar waveguides on sapphire and on bulk silicon was performed to demonstrate the loss behavior of the substrates. The SOS transmission line was fabricated on top of 3000Å of low temperature oxide (LTO), and the SOI transmission line was fabricated on top of 17000Å LTO which was grown on top of a bulk Si wafer. Shown in figure 4 is the comparison of the measured loss characteristics of 50Ω coplanar waveguides. The center conductor of these waveguides are 10µm wide and the spacings to ground are 5.7µm wide. The effective dielectric constants are estimated to be 5.1 and 4.2 for the SOS and bulk case respectively. The loss is

approximately 3 times higher at 10 GHz for the bulk case.

A high impedance waveguide is essential for the gate line matching in order to provide the most inductance per length while minimize the line length. However, higher impedance line would have higher loss due to the larger waveguide to ground plane spacing, enabling in less confinement the electromagnetic wave. EM simulations with SONNET were performed to simulate the maximum impedance line on sapphire. Lossy substrate but lossless metal was assumed. It was found that the maximum impedance without excessive loss (-1 dB) can be achieved for 100Ω waveguide.

For our design, the gate line characteristic impedance is 90Ω and its length per stage is 1.5mm for the 300µm gate width stages. The drain lines are 60Ω line at 1.8 mm for the 300µm stages. The long drain line results in 3Ω of resistance per stage yielding 12Ω of total resistance in the drain line. This degrades the high frequency and high power performance of the distributed amplifiers. Further reduction of drain line resistance is possible in the future with thicker metal deposition or planarized via structures to improve the performance of the distributed amplifiers.

Measured Results

a. Frequency response

The SOS distributed amplifiers were measured on wafer using GGB Picoprobes. The frequency response was measured using the Hewlett Packard HP8510B network analyzer. The best bandwidth was obtained from the design with 300µm per stage and with external terminations which were connected to the probes (Figure 5). The S21 (gain), S11(input matching), and S22 (output matching) are plotted in figure 5.

The VSWR is less than 1.38:1 throughout the operating frequency range. The gain is around 10 dB at low frequencies and up to 2 GHz, 5 dB up to 6 GHz, and 4 dB up to 10GHz. The increase in gain in low frequency was due to the higher impedance of the blocking capacitance at low frequency. The opened drain line termination can peak the low frequency gain. The decrease in gain with frequency over the 5 to 10 GHz range is associated with metal interconnect loss. To the authors' knowledge, the 10 GHz bandwidth is the highest bandwidth for any amplifier implemented with silicon MOSFET technology to date.

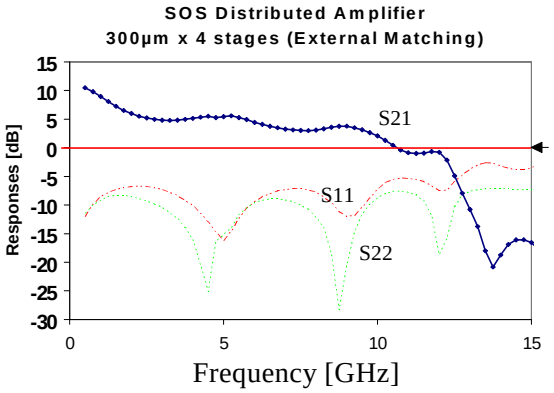

Figure 5. Frequency response of a 4 stage externally matched distributed amplifier (300µm gate width, 4 stages)

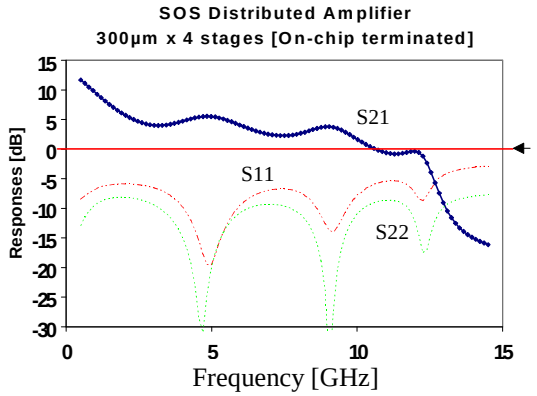

Figure 6. Frequency response of a 4 stage internally matched distributed amplifier (300µm gate width, 4 stages)

The termination elements can also be fabricated on wafer. The blocking capacitors are realized by MIM capacitors. The values for the termination are around 15pF for the drain and the gate lines. They are limited by the area. The termination resistors are made of NiCr thin film technology. Figure 6 shows the result of the on-chip terminated distributed amplifier of the same FETs and coplanar waveguide geometries. The

gain is slightly degraded due to the smaller blocking capacitors.

b. Power Gain

The power gain behavior of a 300µm per stage, external terminated distributed amplifier is

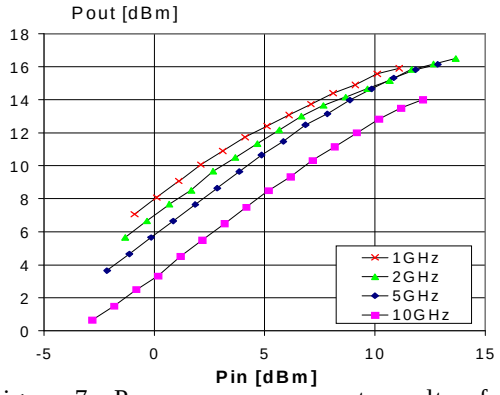

Figure 7. Power measurement results of a 300µm x 4 stage distributed amplifier Vgs=1.2V Vds=2.5V

shown in figure 7. The P_{in} versus P_{out} characteristics show soft saturation behavior. This is due to the metal resistance in the drain line, causing a drop in Vdd for larger power outputs. The maximum power output up to 5 GHz is around 16 dBm, and the power added efficiency (PAE) at that power level is around 12%.

Conclusion

10GHz, 5dB gain distributed amplifiers were realized with silicon on sapphire thin film CMOS technology. Aluminum coplanar waveguides on sapphire were used to provide distributed inductance for interstage matching. The low loss demonstrated by the coplanar waveguides is a key feature that enabled the Si CMOS technology in the RF domain. Currently, the resistance of the aluminum does degrade the performance of the distributed amplifiers and should be optimized in the future.

Acknowledgments

This work is sponsored by ONR 6.2 Microelectronics project, in conjunction with the UCSD NSF Center for High Speed Integrated Circuits and Systems.

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level	3	theta	0.205
tox	1.1e-8	vmax	2.47e5
nsub	0.7e17	kappa	0
vto	0.7	is	1e-16
delta	0	nfs	1e11
uo	410	cj	99u
eta	0.0458	cgso	500p

Table 1. SPICE level 3 model for a L=0.5µm W=100µm NMOS